

CLAIMS

1. A semiconductor storing device in which a row of memory cells is selected by a word line stage and a division word line stage, comprising:
 - memory arrays that each include a plurality of memory cells arranged in a matrix;
 - word lines for respective rows of the memory cells;
 - division word lines each of which is connected to the memory cells arranged in one row corresponding to one word;
 - division word line selectors that select the division word lines, respectively, the division word lines being connected to the respective word lines via the division word line selectors, respectively;
 - pairs of bit lines for reading data from the memory cells and writing data to the memory cells that are connected to the pairs of the bit lines, respectively;
 - column gates connected to the pairs of bit lines, respectively;
 - pairs of data lines that are connected to the pairs of bit lines via the column gates, respectively, to communicate data;
 - write buffers for data writing that are connected to the pairs of data lines, respectively;

sense operational amplifiers for data reading that are connected to the pairs of data lines, respectively; and

data input/output circuits that are connected to the pairs of data lines via the write buffers and the sense
5 operational amplifiers, respectively,

wherein input address data is specified by address data $X[i:0]$, $Y[j:0]$, and $Z[k:0]$, two roots of selection signals for selecting the division word line selectors are provided alternately to the division word lines arranged in
10 one of the memory arrays, and one of the two roots of the selection signals is enabled to select one of the division word line selectors in the one of the memory arrays, and

eight roots of the selection signals in the entire semiconductor storing device are enabled so that when an
15 address (z, y, x) is specified by the input address data $X[i:0]$, $Y[j:0]$, and $Z[k:0]$, eight addresses of (z, y, x) , $(z, y, x+1)$, $(z, y+1, x)$, $(z, y+1, x+1)$, $(z+1, y, x)$, $(z+1, y, x+1)$, $(z+1, y+1, x)$, and $(z+1, y+1, x+1)$ are accessed simultaneously.

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2. The semiconductor storing device according to claim 1, further comprising

selectors that are provided between the write buffers and the data input/output circuits, and between the
25 sense operational amplifiers and the data input/output

circuits, respectively such that the data input/output
circuits always correspond one-to-one to the eight addresses
of (z, y, x) , $(z, y, x+1)$, $(z, y+1, x)$, $(z, y+1, x+1)$, $(z+1, y,$
 $x)$, $(z+1, y, x+1)$, $(z+1, y+1, x)$, and $(z+1, y+1, x+1)$,
5 respectively, and always transmit and receive, via the
selectors, respective input data and output data corresponding
one-to-one to the eight addresses, respectively.

3. The semiconductor storing device according to
10 claim 1, wherein when at least one of z , y , and x of the
address (z, y, x) is an allowable maximum value, at least one
of $z+1$, $y+1$, and $x+1$ that corresponds to the at least one of x ,
 y , and z having the allowable maximum value is converted to
"0" to access the eight addresses simultaneously.

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4. The semiconductor storing device according to
claim 1, further comprising selection means for selecting
either a first mode in which the eight addresses are accessed
simultaneously, or a second mode in which a single address is
20 accessed.

5. A semiconductor storing device in which a row
of memory cells is selected by a word line stage and a
division word line stage, comprising:

25 memory arrays that each include a plurality of

memory cells arranged in a matrix;

word lines for respective rows of the memory cells;

division word lines each of which is connected to
the memory cells arranged in one row corresponding to one

5 word;

division word line selectors that select the
division word lines, respectively, the division word lines
being connected to the respective word lines via the division
word line selectors, respectively;

10 pairs of bit lines for reading data from the memory
cells and writing data to the memory cells that are connected
to the pairs of the bit lines, respectively;

column gates connected to the pairs of bit lines,
respectively;

15 pairs of data lines that are connected to the pairs
of bit lines via the column gates, respectively, to
communicate data;

write buffers for data writing that are connected
to the pairs of data lines, respectively;

20 sense operational amplifiers for data reading that
are connected to the pairs of data lines, respectively; and

data input/output circuits that are connected to
the pairs of data lines via the write buffers and the sense
operational amplifiers, respectively,

25 wherein input address data is specified by address

data $X[i:0]$, $Y[j:0]$, and $Z[k:0]$, four roots of selection signals for selecting the division word line selectors are provided to the division word lines arranged in one of the memory arrays, and one of the four roots of the selection
5 signals is enabled to select one of the division word line selectors in the one of the memory arrays, and

eight roots of the selection signals in the entire semiconductor storing device are enabled so that when an address (z, y, x) is specified by the input address data
10 $X[i:0]$, $Y[j:0]$, and $Z[k:0]$, eight addresses of (z, y, x) , $(z, y, x+1)$, $(z, y+1, x)$, $(z, y+1, x+1)$, $(z+1, y, x)$, $(z+1, y, x+1)$, $(z+1, y+1, x)$, and $(z+1, y+1, x+1)$ are accessed simultaneously.

15 6. The semiconductor storing device according to claim 5, further comprising

selectors that are provided between the write buffers and the data input/output circuits, and between the sense operational amplifiers and the data input/output
20 circuits, respectively such that the data input/output circuits always correspond one-to-one to the eight addresses of (z, y, x) , $(z, y, x+1)$, $(z, y+1, x)$, $(z, y+1, x+1)$, $(z+1, y, x)$, $(z+1, y, x+1)$, $(z+1, y+1, x)$, and $(z+1, y+1, x+1)$, respectively, and always transmit and receive, via the
25 selectors, respective input data and output data corresponding

one-to-one to the eight addresses, respectively.

7. The semiconductor storing device according to claim 5, wherein in a case where when the address (z, y, x) is specified, an address determined by at least one of z+1, y+1, and x+1 does not exist in the semiconductor storing device, the at least one of z+1, y+1, and x+1 is converted to "0" to access the eight addresses simultaneously

8. The semiconductor storing device according to claim 5, further comprising selection means for selecting either a first mode in which the eight addresses are accessed simultaneously, or a second mode in which a single address is accessed.

9. A semiconductor storing device in which a row of memory cells is selected by a word line stage and a division word line stage, comprising:

memory arrays that each include a plurality of memory cells arranged in a matrix;
word lines for respective rows of the memory cells;
division word lines each of which is connected to the memory cells arranged in one row corresponding to one word;

division word line selectors that select the

division word lines, respectively, the division word lines being connected to the respective word lines via the division word line selectors, respectively;

5 pairs of bit lines for reading data from the memory cells and writing data to the memory cells that are connected to the pairs of the bit lines, respectively;

 column gates connected to the pairs of bit lines, respectively;

10 pairs of data lines that are connected to the pairs of bit lines via the column gates, respectively, to communicate data;

 write buffers for data writing that are connected to the pairs of data lines, respectively;

15 sense operational amplifiers for data reading that are connected to the pairs of data lines, respectively; and

 data input/output circuits that are connected to the pairs of data lines via the write buffers and the sense operational amplifiers, respectively,

20 wherein input address data is specified by address data $X[i:0]$, $Y[j:0]$, and $Z[k:0]$, two roots of selection signals for selecting the division word line selectors are provided alternately to the division word lines arranged in one of the memory arrays, and one of the two roots of the selection signals is enabled to select one of the division
25 word line selectors in the one of the memory arrays, and

four roots of the selection signals in the entire semiconductor storing device are enabled so that when an address (z, y, x) is specified by the input address data X[i:0], Y[j:0], and Z[k:0], four addresses of (z, y, x), (z, y, x+1), (z, y+1, x), and (z, y+1, x+1) are accessed simultaneously.

10. The semiconductor storing device according to claim 9, further comprising

10 selectors that are provided between the write buffers and the data input/output circuits, and between the sense operational amplifiers and the data input/output circuits, respectively such that the data input/output circuits always correspond one-to-one to the four addresses of

15 (z, y, x), (z, y, x+1), (z, y+1, x), and (z, y+1, x+1), respectively, and always transmit and receive, via the selectors, respective input data and output data corresponding one-to-one to the four addresses, respectively.

20 11. The semiconductor storing device according to claim 9, wherein in a case where when the address (z, y, x) is specified, an address determined by at least one of z+1, y+1, and x+1 does not exist in the semiconductor storing device, the at least one of z+1, y+1, and x+1 is converted to "0" to

25 access the four addresses simultaneously.

12. The semiconductor storing device according to
claim 9, further comprising selection means for selecting
either a first mode in which the four addresses are accessed
5 simultaneously, or a second mode in which a single address is
accessed.